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Real-Time Controller Design Test Bench for High-Voltage Direct Current Modular Multilevel Converters

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Abstract: Modular multilevel converters (MMCs), with their inherent features and advantages over other conventional converters, have gained popularity and remain an ongoing topic of research. Many scholars have solved issues related to the operation, control, protection, and reliability of MMCs using simulation software and small hardware prototypes. We propose a novel approach for an MMC controller design with real-time systems. By utilizing a key benefit of LabVIEW Multisim co-simulation, an MMC control algorithm that can be deployed on a field-programmable gate array (FPGA) was developed in LabVIEW. The complete circuit was designed in Multisim, and a co-simulation was performed to drive an MMC model. The benefit of this topology is that control algorithms can be designed in a LabVIEW FPGA and tested with the Multisim co-simulation circuit to obtain simulation results. Once the controller works and provides satisfactory results, the same algorithm can be deployed in any NI (National Instruments) FPGA-based controller, like a compact remote input/output (RIO), to control real-time MMCs designed in an NI PCI eXtensions for Instrumentation (PXI) system. This method saves time and provides flexibility for effectively designing control algorithms and implementing them in an FPGA for real-time model implementation.

Keywords: modular multilevel converter; MMC co-simulation; hardware-in-loop; HVDC; real-time controller

1. Introduction

With increasing global warming, renewable energy sources are being used to generate power. Offshore wind turbines, because of the more linear wind velocity profile, are an example of a renewable energy source; however, they are located far away from load centers [1]. In transmitting power to load centers, high-voltage direct current (HVDC) transmission lines are preferred over high-voltage alternating current (HVAC) lines because they require fewer conductors and have less power losses, no skin effect, a reduced right of way, and good stability [2,3].

Modular multilevel converters (MMCs) are ideal converter topologies used for interfacing between HVDC and HVAC transmission systems. Compared with conventional converters, MMCs are more advantageous because they have modularity, scalability in terms of voltage and current, redundancy, good reliability, independent control of active and reactive power, low switching frequency, low total harmonic distortion (THD) in the output waveforms, and no filter requirement [4]. The first MMC HVDC was commissioned in December 2013 on Nan'ao Island, and another MMC HVDC system was installed on the Zhoushan Islands, China [5].

Many researchers are studying design control schemes for MMCs. For instance, the authors in [6] developed a simplified capacitor voltage balancing technique that does not require sorting to select submodules. In [7], the circulating currents of MMCs were controlled using an adaptive proportional integral (API) controller to reduce secondary harmonic components, and its performance was measured and compared with a proportional resonant (PR) controller for transient response, stability, optimal performance, and reference tracking in MATLAB. The authors in [8] proposed an energy-balancing control strategy to keep an MMC operating normally under submodule (SM) fault conditions in which PSCAD was used to simulate the system, and a small prototype was used to validate the results. A novel control strategy for MMCs based on differential flatness theory was proposed in [9]. Their results highlight the capability of the proposed controller in steady and dynamic conditions while maintaining MMC currents and voltages by controlling active and reactive power. Several researchers have developed small prototypes to verify their control algorithms. The algorithms are developed early in the simulation process and need to be written for the controller chosen to run the prototype, which takes time and effort and is costly [10–21]. As an emerging technology, there are few tools for MMC controller design and no established standards to guide engineering practices for MMC control and operation. Thus, there is a need for a platform where control algorithms are designed once and can be utilized for simulation and real-time implementation, ultimately saving time during the development and testing of the system.

This study presents a development platform using a LabVIEW Multisim co-simulation (Figure 1) that can develop control algorithms in a graphical-language-based LabVIEW platform for MMC simulation and allows the same program to be used for the control of the real-time MMC system implemented in a National Instruments (NI) PCI eXtensions for Instrumentation (PXI) system. In LabVIEW Multisim co-simulation, the control algorithm is designed with a LabVIEW field-programmable gate array (FPGA), and the circuit is developed in Multisim. Using the control algorithm, the circuit can be operated with the controls designed in LabVIEW. Therefore, the proposed real-time controller design test bench for HVDC MMCs saves time, money, and effort required for the development and testing of the system.

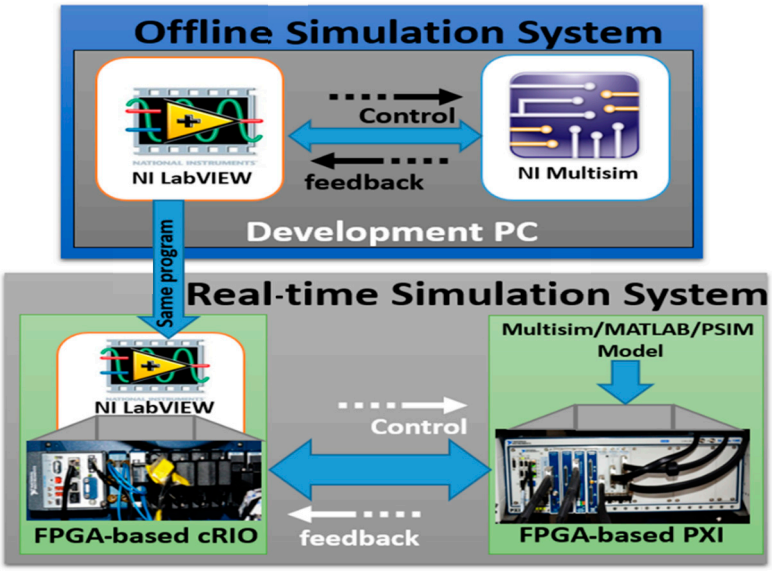


Figure 1. LabVIEW Multisim co-simulation block diagram.

2. Comparison with Conventional Methods

Andrus et al. [22] studied a test bed design for HVDC systems to design fault management with a scaled-down MMC with a full bridge, but their system cannot be extended further due to hardware limitations. The work presented in [23] demonstrates a real-time simulation of an MMC-based MVDC

traction system in which an FPGA-based system is used for real-time simulation. Additionally, a second offline simulation, PSCAD/EMTDC, was used for simulation and real-time verification of the results. The authors of [24] presented a 5 MW test bed hardware setup where the simulation results were verified from the test bed; however, the hardware was put at risk. In [25], a small prototype was developed with 10 SMs in each arm, and control algorithms were developed for a system with NI controllers. However, the system was limited to only 10 SMs, so the simulation results were obtained with different software. Several other studies [26–28] presented test beds for HVDC systems, but their systems either limited or lacked simulation verification without changing the control algorithm.

3. Operating Principles and Mathematical Modelling of the Proposed Controller Design Test Bench for the HVDC MMC

The single-phase topology of the MMC is shown in Figure 2a, which is composed of one phase/arm. The phase is further divided into an upper arm and a lower arm connected together by inductors. Each arm has N connected submodules (SMs) (SM1, SM2, etc.) in series, and each SM consists of two switches and a capacitor connected across them. By applying Kirchhoff's voltage law (KVL) in the upper and lower loops, as shown in Figure 2a, we obtain

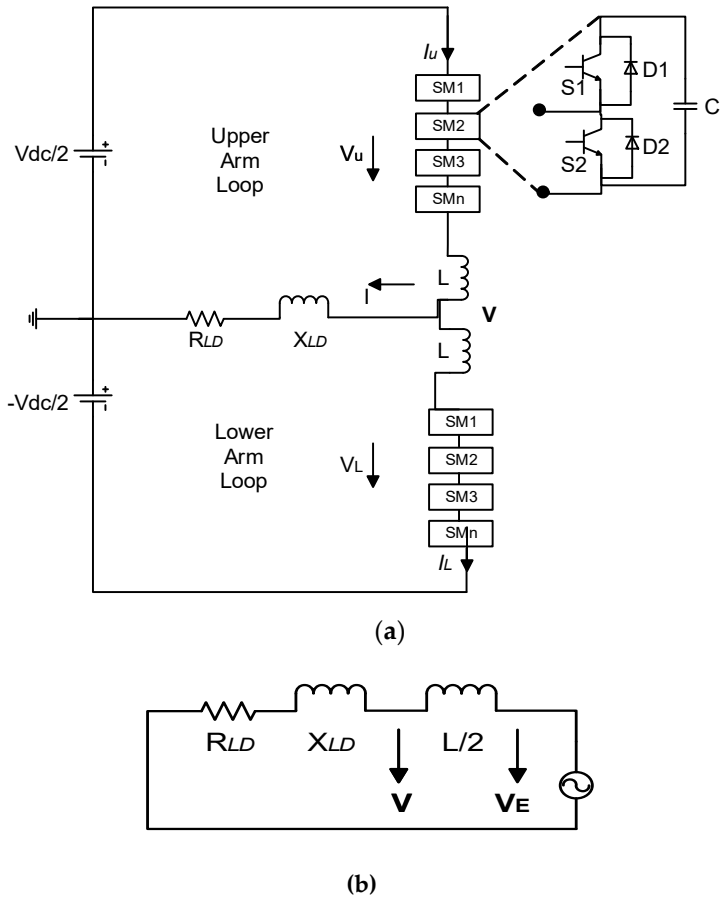


Figure 2. (**a**) Single-phase modular multilevel converter (MMC) circuit diagram; (**b**) equivalent circuit of the MMC.

$$V = \frac{1}{2}V_{dc} - V_u - L\frac{di_U}{dt} \tag{1}$$

$$V = -\frac{1}{2}V_{dc} + V_L + L\frac{di_L}{dt} \tag{2}$$

Then we apply Kirchhoff's current law (KCL) to obtain the output current:

$$i = i_L + i_U \tag{3}$$

The equivalent circuit of the MMC is shown in Figure 2b. Using Equations (1) and (2), the output voltage is

$$V = \frac{1}{2}(V_L - V_U) + \frac{L}{2}\frac{di}{dt} \tag{4}$$

It is clear from Equation (3) that the equivalent inner voltage of the phase can be expressed as

$$V_E = \frac{1}{2}(V_L - V_U) \tag{5}$$

Generally, the V_E can be shown as

$$V_E^{ref} = \frac{mV_{dc}}{2}\cos(\omega t) \tag{6}$$

where m is the modulation index with $0 < m < 1$ and ω is the angular frequency. N submodules are used in the circuit with conventional NLM methods, so Equation (7) is satisfied on the DC side.

$$V_{dc} = V_L + V_U \tag{7}$$

Reference voltages for the upper and lower arms can be expressed as

$$V_U^{ref} = \frac{V_{dc}}{2}[1 - m\cos(\omega t)] \tag{8}$$

$$V_L^{ref} = \frac{V_{dc}}{2}[1 + m\cos(\omega t)] \tag{9}$$

The circulating currents flowing due to the voltage difference in each arm can be found by Equations (10)–(12). These currents distort the leg current, produce additional heat in the switches, increase the rated current of power devices, and cause loss in the MMC. They must be controlled and reduced to avoid losses and reduce system cost.

$$i_U = i_{circ} + \frac{i}{2} \tag{10}$$

$$i_L = i_{circ} - \frac{i}{2} \tag{11}$$

$$i_{circ} = \frac{i_U + i_L}{2} \tag{12}$$

Equations (1) and (2) provide an understanding of the operation of the MMC. The SM voltages should be equal to $\frac{1}{2}\ V_{dc}$ with the total DC link voltage V_{dc}. Consider a basic three-level MMC with two SMs in the upper arm and two in the lower arm. When one SM is inserted in each arm, using Equations (1) and (2), we will get zero.

Similarly, when all the SMs in the lower arm are inserted and the SMs in the upper arm are bypassed, we will get an output voltage of $\frac{1}{2}\ V_{dc}$. When all the SMs in the upper arm are inserted, and the SMs in the lower arm are bypassed, we will obtain $-\frac{1}{2}\ V_{dc}$. In case of an even number of levels, a zero output voltage cannot be obtained. The switching pattern of the SMs is shown in Table 1, and the waveform is displayed in Figure 3a.

Table 1. Switching pattern of the submodules (SMs) for a 3-level MMC.

1-Phase	SM Number	Output Voltage Levels						
		0	$\frac{1}{2}V_{dc}$	0	$-\frac{1}{2}V_{dc}$	0	$\frac{1}{2}V_{dc}$	0
Upper Arm	SM1	✓	×	✓	✓	✓	×	✓
	SM2	×	×	×	✓	×	×	×
Lower Arm	SM1	✓	✓	✓	×	✓	✓	✓
	SM2	×	✓	×	×	×	✓	×

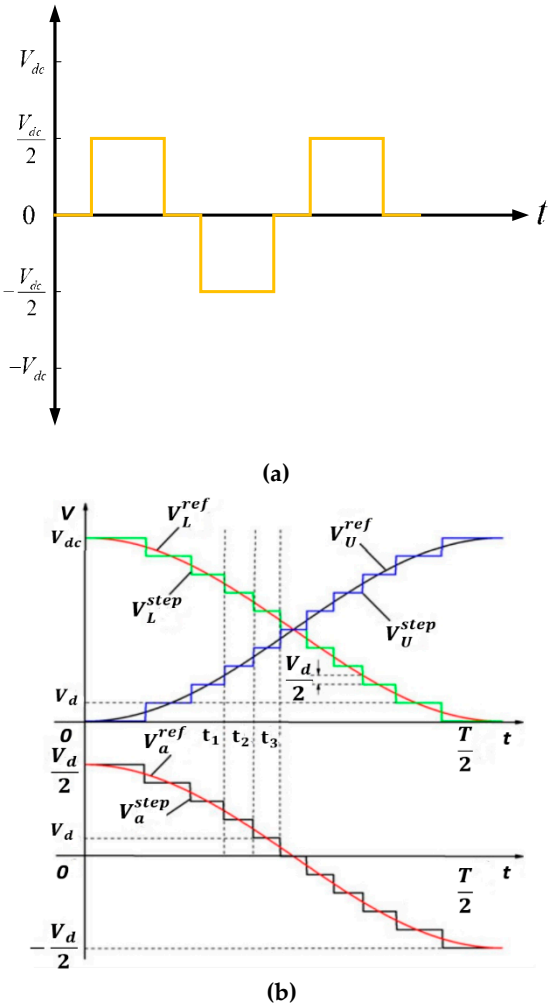


Figure 3. (**a**) Switching pattern of the output waveform; (**b**) switching states of the reference and output waveform.

We can conclude from the switching pattern that when all the SMs in the lower arm are inserted and the SMs in the upper arm are bypassed, we will observe a positive peak voltage. Similarly, when all the SMs in the upper arm are inserted and the SMs in the lower arm are bypassed, we will observe negative peaks in the output waveform. Using this concept, we can develop a switching pattern for any number of levels.

4. Proposed LabVIEW Multisim Co-Simulation Platform

LabVIEW is a graphical programming language that enables us to program the FPGA without using VHDL or Verilog. A nearest level control (NLC) algorithm was developed in LabVIEW to control the MMC operation and was compatible for deployment in real-time NI controllers (i.e., compact reconfigurable input/output (cRIO)). NLC is advantageous because the algorithm does not require complex changes when output waveform levels are increased for power quality analysis. Equations (13) and (14) are used to implement the NLC algorithm, where, V_d is the capacitor voltage, V_{dc} is the total DC link voltage, and N_U and N_L determine the total number of SMs to be inserted at any instant in the upper and lower arm, respectively.

$$N_U = round_{0.5}\frac{V_{dc}}{2V_d}(1 + m\cos(\omega t)) \tag{13}$$

$$N_L = round_{0.5}\frac{V_{dc}}{2V_d}(1 - m\cos(\omega t)) \tag{14}$$

4.1. Open-Loop Results of MMC Co-Simulation

The open-loop NLC-based algorithm developed in LabVIEW for co-simulation is shown in Figure 4.

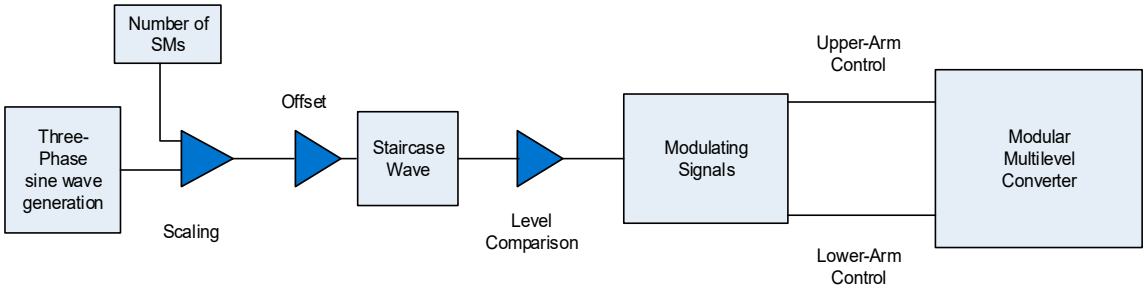


Figure 4. Open-loop control algorithm development in LabVIEW for the MMC.

The inserted number of SMs can be calculated by Equations (13) and (14). The round function $round_{0.5}$ (x) will round the real number x to the nearest whole number according to the decimal fraction of x. If the decimal fraction of x is greater than 0.5, x is rounded up to the next whole number, or else it is rounded down to the next whole number. To understand the switching states, two cases [t_1 to t_2, t_2 to t_3] are analyzed and shown in Figure 3b. In the first case [t_1 to t_2], assuming $V_L^{step} = MV_d$, then the reference values of the arm voltages and equivalent inner voltage of the phase at t = t_1 can be shown as Equations (15) and (16), respectively.

$$\begin{cases} V_L^{ref} = (M + 0.5)V_d \\ V_U^{ref} = [(N - M - 1) + 0.5]V_d \end{cases} \tag{15}$$

$$V_E^{ref} = (M - 0.5N + 0.5)V_d \tag{16}$$

In the first scenario, the step waves of the arm voltages and equivalent inner voltage are expressed as

$$\begin{cases} V_L^{step} = MV_d \\ V_U^{step} = (N - M)V_d \end{cases} \tag{17}$$

$$V_E^{step} = (M - 0.5N)V_d \tag{18}$$

In the second scenario, from t_2 to t_3, the reference values of the arm voltages and equivalent inner voltage are expressed as

$$\begin{cases} V_L^{ref} = [(M-1)+0.5]V_d \\ V_U^{ref} = [(N-M)+0.5]V_d \end{cases} \quad (19)$$

$$V_E^{ref} = (M-0.5N-0.5)V_d \quad (20)$$

The step waves of the arm voltages and equivalent inner voltage are shown as

$$\begin{cases} V_L^{step} = (M-1)V_d \\ V_U^{step} = (N-M+1)V_d \end{cases} \quad (21)$$

$$V_E^{step} = (M-0.5N-1)V_d \quad (22)$$

Comparing Equations (18) and (22), it can be observed that the step height in V_E^{step} is V_d. Since the positive and negative DC voltage limits are $\pm 0.5V_{dc}$, the maximum level in the equivalent inner voltage is equal to V_{dc}/V_d +1.

The solver methods recommended for co-simulation are R-K 23 and 45 ODE solvers since they can auto-adjust the rate of the loop according to the complexity of the circuit. The MMC model was designed in the NI Multisim software, and a half-bridge SM topology was considered for co-simulation. The sub-circuit for each arm was made as shown in Figure 5. An open simple RL load is considered for co-simulation.

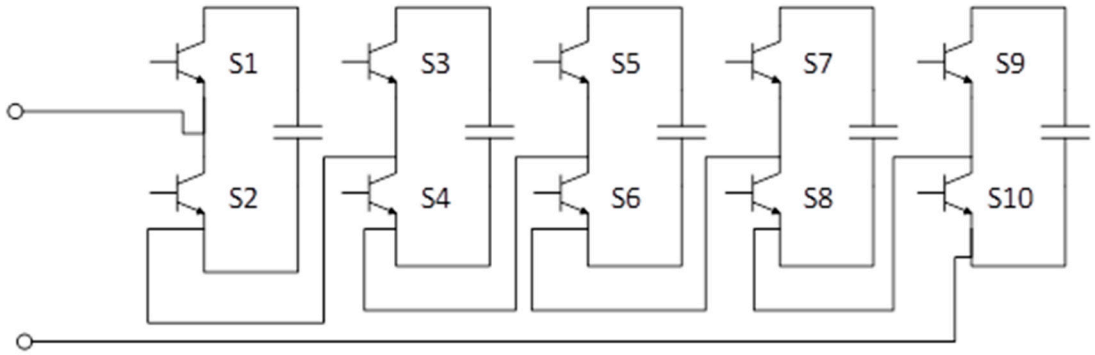


Figure 5. Sub-circuit of each arm in National Instruments (NI) Multisim.

Each arm is an MMC that is connected by inductors to reduce the current change when all the SMs in the arm are bypassed and to limit the fault current. In Multisim, on-page connectors are used to distribute the signals coming from LabVIEW since only 24 inputs/outputs are allowed in LabVIEW Multisim co-simulation; however, they can be increased using decoders. The MMC circuit designed in Multisim is shown in Figure 6.

The open-loop MMC co-simulation was completed using an NLC control algorithm to obtain the results, and a simple RL load was considered. Capacitor voltage balancing was not considered. The output voltage waveform and current are shown in Figure 7.

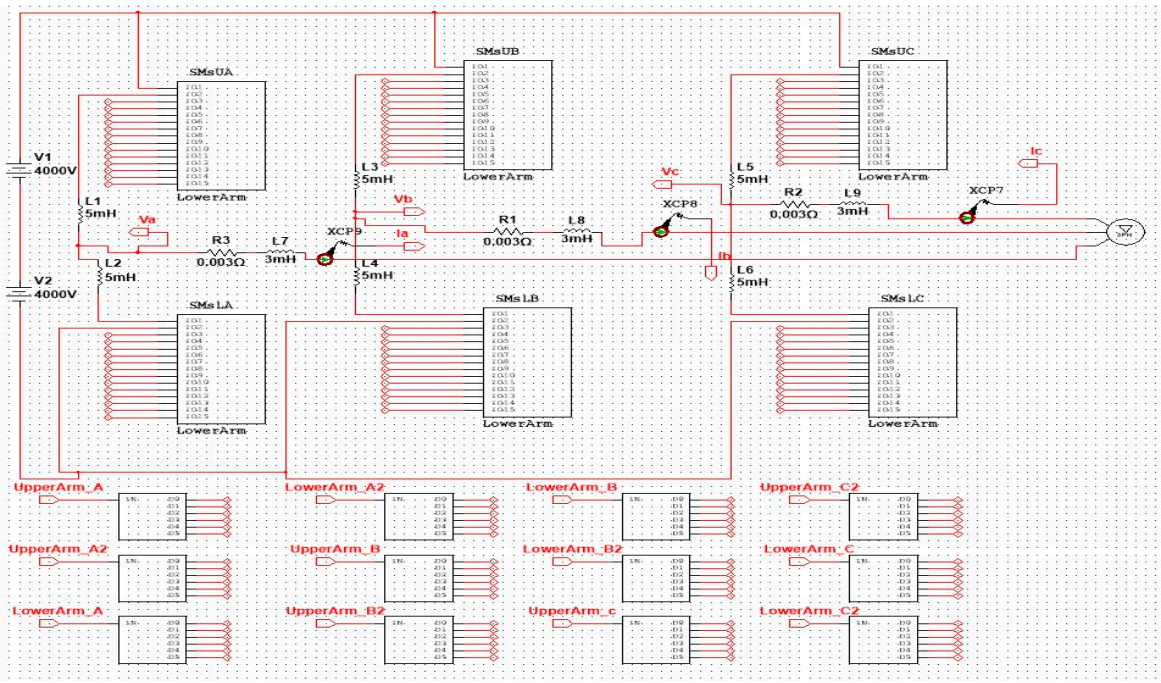
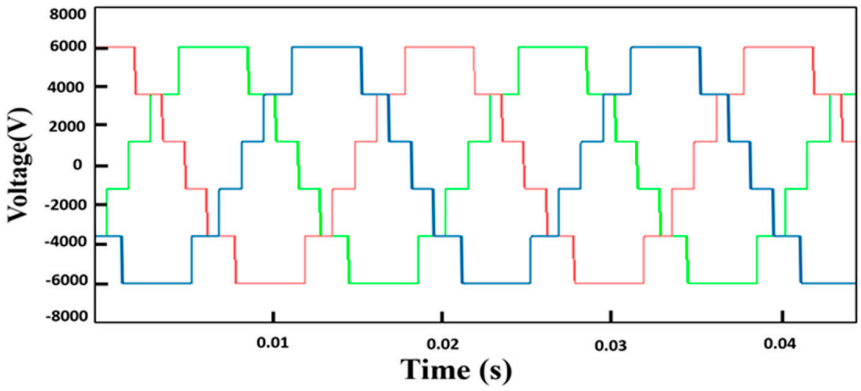
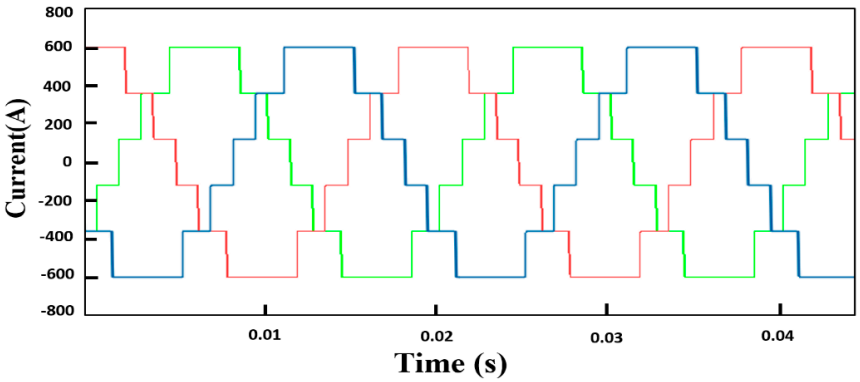


Figure 6. MMC circuit designed in NI Multisim.



(a)



(**b**)

Figure 7. Three-phase 6-level output (**a**) voltage and (**b**) current waveforms of the MMC.

4.2. Closed-Loop NLC Algorithm Design in LabVIEW

Modulation signals must be controlled and varied accordingly to control active and reactive power in a closed-loop MMC as depicted in Figure 8. The modulation signals are sinusoids and cannot be controlled instantaneously; therefore, two frames of reference are used: a stationary frame of reference or the alpha–beta frame, and a rotating frame of reference or the DQ frame. In LabVIEW, the DQ frame is used to achieve zero steady state errors with a pi controller.

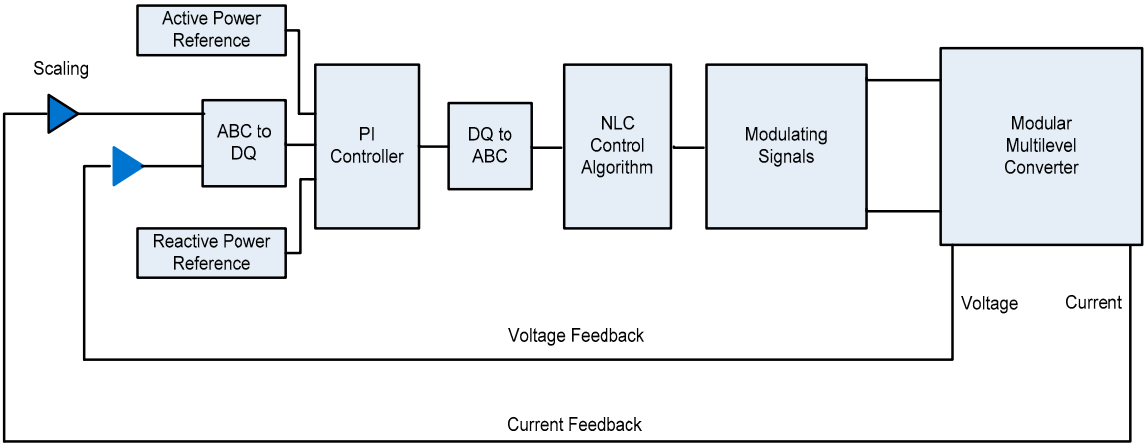


Figure 8. Closed-loop control algorithm development in LabVIEW for the MMC.

Capacitor voltages in the MMC are not constant and need to be measured continuously whenever an SM is inserted or bypassed according to the direction of the arm current and value of the capacitor voltage. When the arm current is positive, capacitors are sorted from lowest to highest voltage, and capacitors with low voltages are inserted so they can be charged. In contrast, when the arm current is negative, capacitors are sorted from highest to lowest voltage, and the capacitors with high voltages are inserted so they can be discharged. In this experiment, the capacitor voltages were considered constant, and no voltage balancing algorithm was applied.

The output voltage and current were measured from the Multisim model node in LabVIEW as shown in Figure 9; Figure 10, respectively. In a closed-loop system, the output of the MMC is tied with the voltage source equivalent to grid. These measured parameters are fed back to the controller for active and reactive power control. The DQ reference frame was used to achieve zero steady state error.

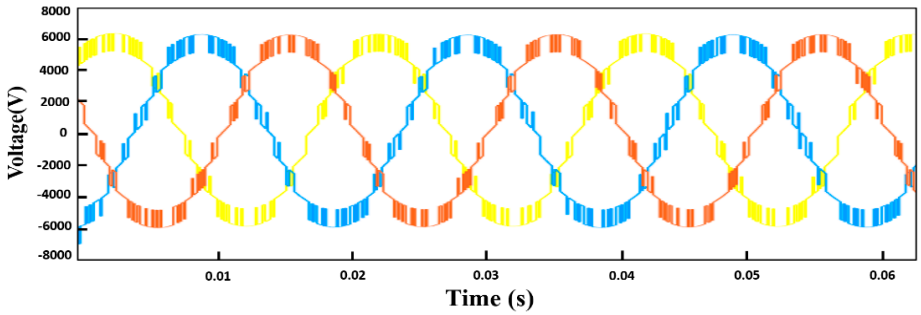


Figure 9. Output voltage of the closed-loop MMC LabVIEW Multisim co-simulation.

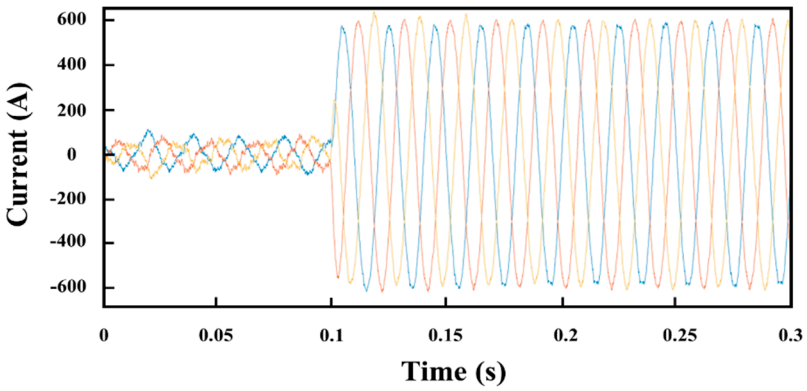


Figure 10. Output current flowing into grid.

The active and reactive power controls were enabled at 0.1 s, and the observed response is shown in Figures 11 and 12, respectively. The circulating current flowing in each phase of the MMC was found using Equation (12) and is shown in Figure 13, and it flows due to the potential difference between the upper and lower arm caused by the difference in SM capacitor voltage. Its magnitude must be reduced to zero in order to avoid losses in the MMC. Increasing the arm inductance decreases the circulating current but does not eliminate it. Its negative sequence component rotates at twice the line frequency. Different types of faults (i.e., line-to-line fault and three-phase fault) are also analyzed and shown in Figures 14 and 15, respectively. The converter parameters are shown in Table 2.

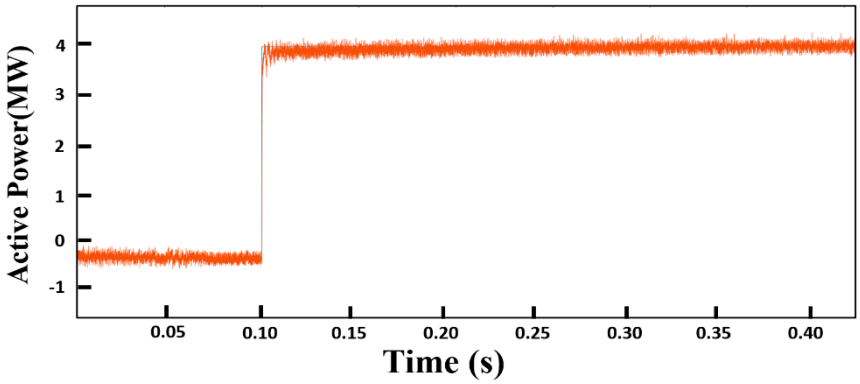


Figure 11. Active power control of the MMC in the LabVIEW Multisim co-simulation.

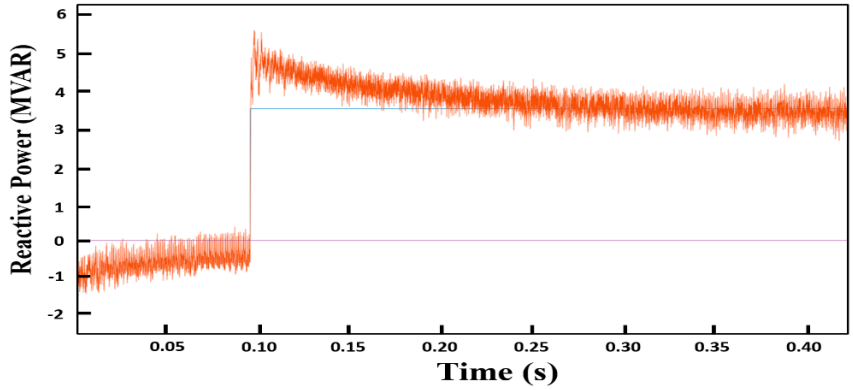


Figure 12. Reactive power control of the MMC in the LabVIEW Multisim co-simulation.

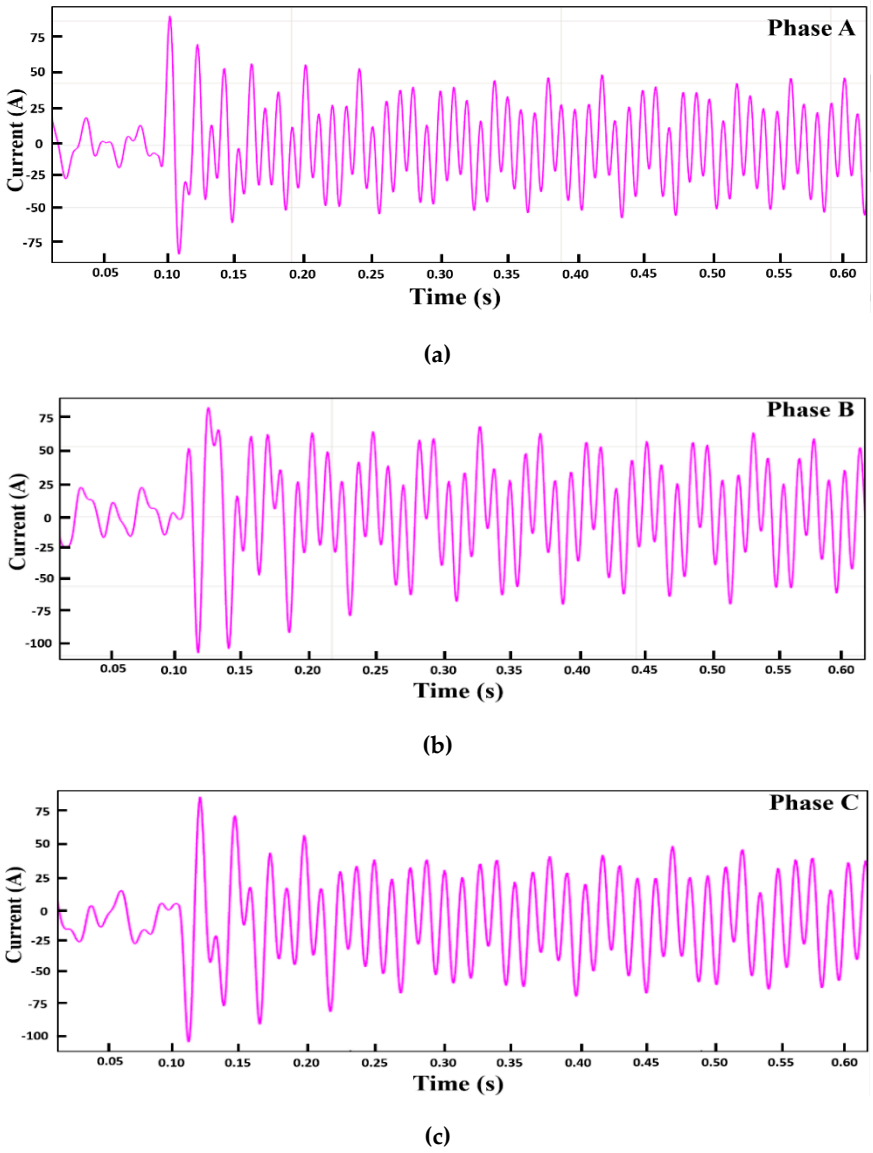


Figure 13. Circulating current flowing in each phase of the MMC: (**a**) phase A, (**b**) phase B, and (**c**) phase C.

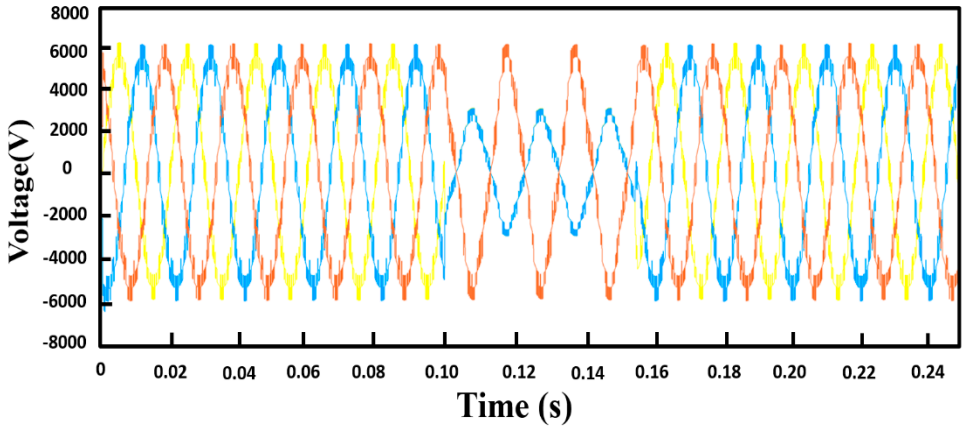


Figure 14. Line-to-line fault.

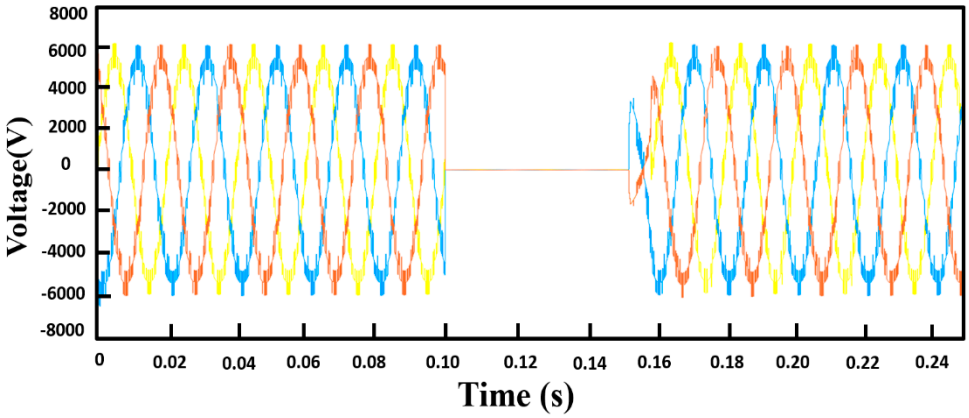


Figure 15. Three-phase symmetrical fault.

Table 2. System parameters and values.

Item No.	System Parameters	Values
1	Rated power	10 MVA
2	Vac grid voltage	4.16 kV
3	V_{dc}	8 kV
4	Switching frequency	300 Hz
5	Rated frequency	50 Hz
6	SM_cap (submodule capacitance)	5000 μF
7	L_arm (arm inductance)	5 mH
8	L_val (line inductance)	3 mH
9	R_line (line resistance)	0.003 Ω

5. Real-Time Control Algorithm Implementation and Testing in NI Compact RIO and PXIe

The compact RIO (cRIO) combines an RT operating system with an embedded floating-point processor. It has a remarkable FPGA performance and hot-swappable analogue and digital input/output modules with hardware flexibility. Each module in cRIO is directly connected to the FPGA, imparting minimum jitter and high-speed input/output signal processing. The FPGA is physically linked to the RT processor via a PCI bus as shown in Figure 16, which represents the internal architecture of the cRIO with an open retrieve to basic hardware resources. The FPGA and RT processor are programmed in LabVIEW, which is a graphical-language-based programming platform. LabVIEW has integrated data-fetching mechanisms to circulate data from the FPGA to the input/output modules and from the FPGA to the RT processor for real-time analysis, data logging, post-processing, and communication with the host computer.

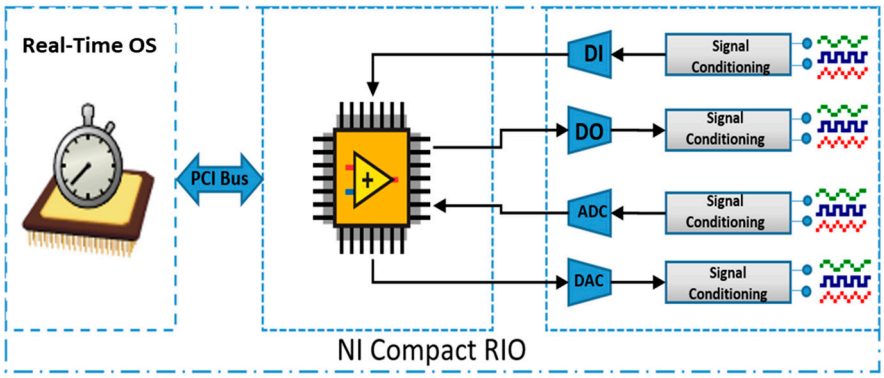


Figure 16. NI compact reconfigurable input/output (cRIO) architecture.

The control algorithm designed in LabVIEW was first compiled through the NI cloud servers and then downloaded in the NI cRIO FPGA to see the actual behavior of the controller. The algorithm was tested at different levels of the MMC, as shown in Figure 18. The system setup is shown in Figure 17, and the results obtained from the cRIO are shown in Figure 18; Figure 19. Once the controller showed the desired behavior, the signals generated from the cRIO were used to operate a real-time MMC circuit implemented in an NI FPGA-based PXIe system. The results obtained from the PXIe system are shown in Figure 20; Figure 21 and can be compared with the initially obtained results from the co-simulation.

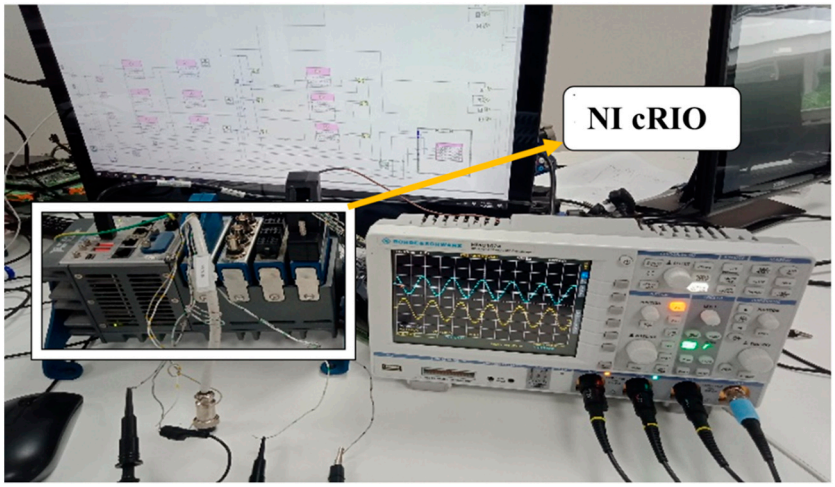
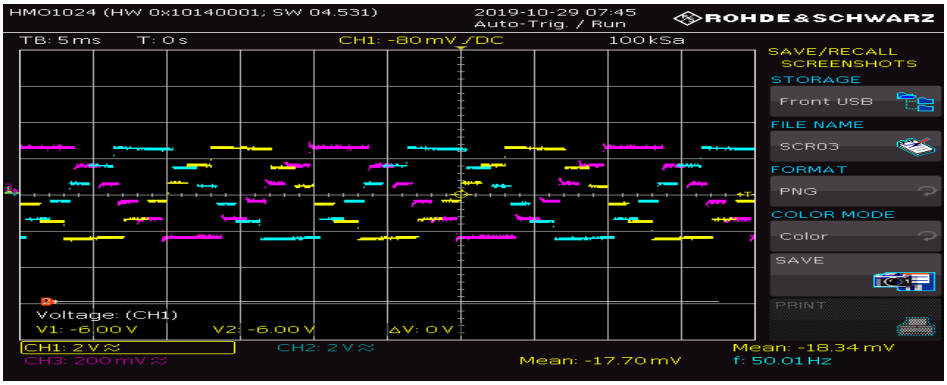
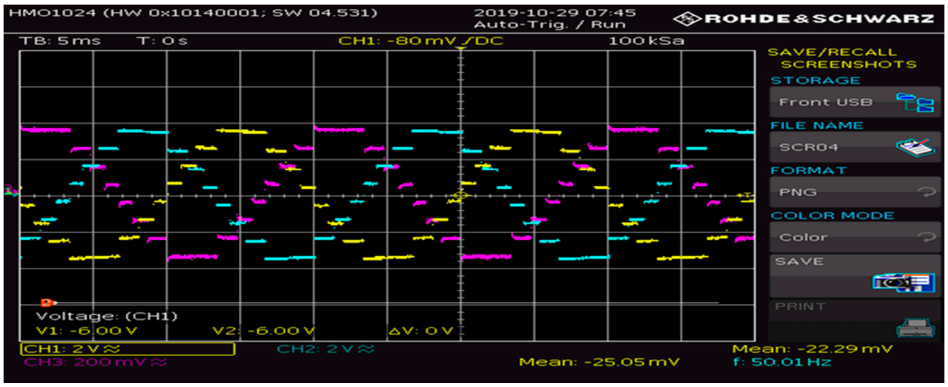


Figure 17. NI cRIO-based setup for real-time control algorithm testing.



(a)



(b)

Figure 18. (**a**) 6-level MMC control staircase waveform; (**b**) eight-level MMC control staircase waveform.

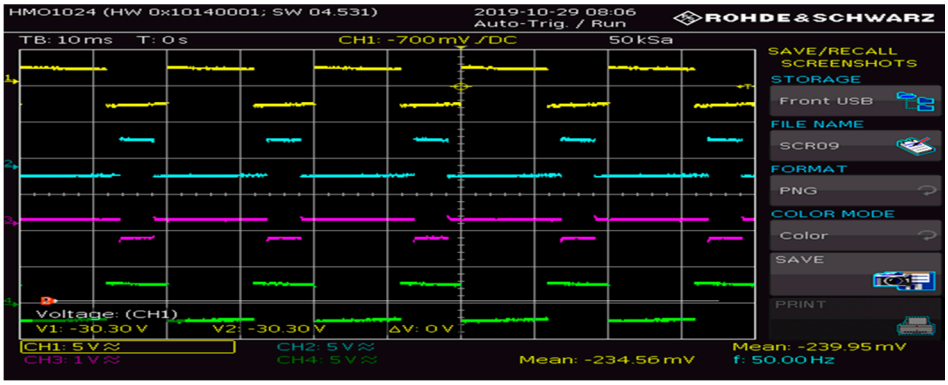


Figure 19. Switching signal for SM operation in the MMC.

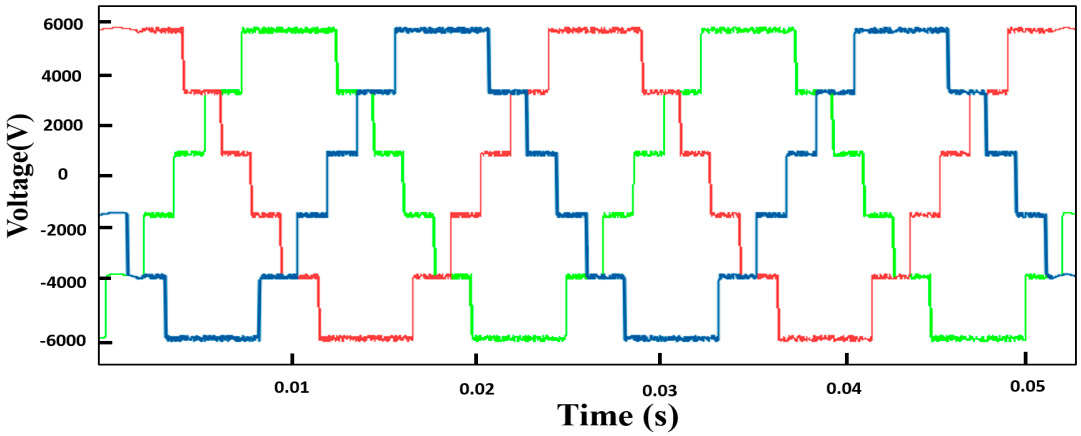


Figure 20. Three-phase 6-level output voltage from PXIe.

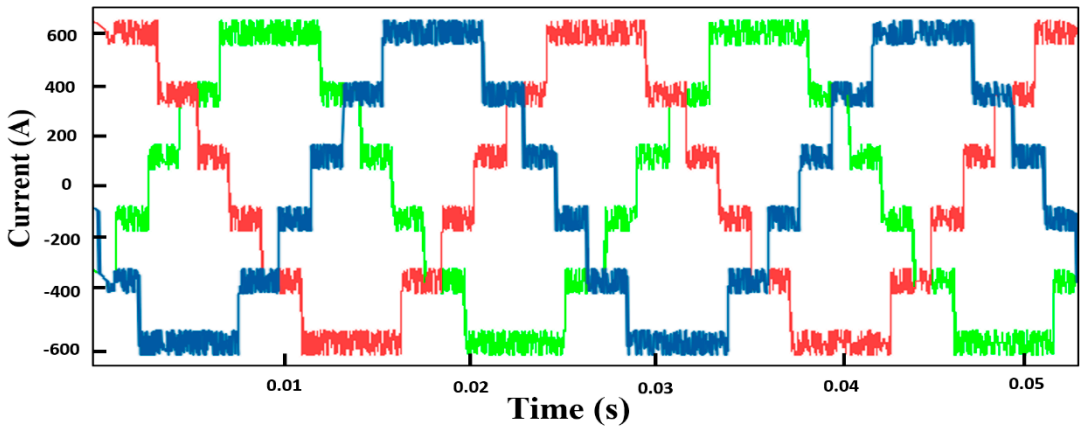


Figure 21. Three-phase 6-level output current from PXIe.

6. State-of-the-Art Hardware-in-Loop Setup

The hardware-in-loop (HIL) architecture helps the user to build a model in MATLAB/PLECS/PSIM/Multisim and burn it into PXI through an eHS solver provided by OPAL RT, which is an FPGA-based floating-point solver that helps the user to burn an electrical circuit on the FPGA automatically with a step size of 250 nanoseconds and without having to code in VHDL or calculating system equations. In our case, the minimum time step at which a model is loaded in PXI is 480 nanoseconds. The overall scheme of the RT system discussed above is shown in Figure 22. Initially, the co-simulation was performed using LabVIEW and Multisim on a desktop PC. After obtaining the results, the same developed algorithm on LabVIEW was burned on an FPGA-based real-time controller

cRIO as shown in Figure 22. After getting satisfactory results from the controller, the real simulation was performed using an actual controller and PXIe system.

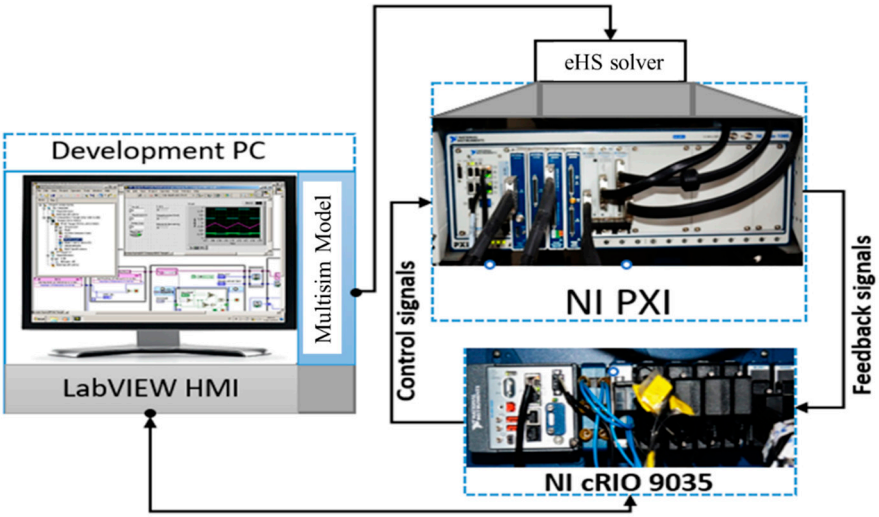


Figure 22. Experimental setup of hardware-in-loop (HIL) architecture.

However, the total number of switches that can be used in one model is limited to 72 in PXIe. Additionally, there is a total of 64 analogue outputs that can be used as an input feedback to the controller cRIO from PXI.

7. Conclusions

Owing to an increased interest in HVDC MMCs, a platform where control algorithms are developed for simulations and deployed after the verification of the simulation results without changing the designed code is needed. In this study, a LabVIEW Multisim co-simulation platform was presented for designing a control algorithm that could be used to run the MMC circuit designed in Multisim and provide the simulation results. Now, once the simulation results are verified, the same algorithm can be loaded to NI controllers, such as the NI cRIO or myRIO, and the real-time controller can be used to control the real-time MMC burned in PXIe, which is a real-time digital simulator. Therefore, the use of this platform allows for obtaining simulation results and does not require changes to the code for real-time applications.

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